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VERIFICATION OF A TRANSLATION

Assistant Commissioner for Patents
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2. That I am knowledgeable in the English language and in the language of JP2002-064893, and I believe the attached English translation to be a true and complete translation of JP2002-064893.

3. The document for which the attached English translation is being submitted is a patent application on an invention entitled PLASMA DISPLAY APPARATUS.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: December 12, 2005

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[Title of the Invention] Plasma Display System

[Claims]

[Claim 1] A plasma display system comprising: a panel section having a substrate formed with a plurality of scanning electrodes and sustaining electrodes in pairs and a substrate formed with data electrodes disposed perpendicularly of the scanning electrodes and retaining electrodes, in which the substrates are opposed to each other, and a drive unit which outputs a driving voltage for driving the panel section, wherein waveforms of the driving voltage include a sustaining period of alternately applying a sustaining pulse voltage for sustaining discharge to the scanning electrode and the sustaining electrode and an erasing period of applying an oblique waveform voltage different in polarity from the sustaining pulse voltage to an electrode different from the electrode to which final sustaining pulse voltage is applied.

[Claim 2] The plasma display system of claim 1, wherein the final sustaining pulse voltage is positive, and minimum voltage Vnr (V) of the oblique waveform voltage in the erasing period has a relationship with discharge start voltage Vf1 (V) between an oblique waveform voltage input electrode and a data electrode such as follows:

$$-(Vf1 - 60) \leq Vnr \leq -30$$

[Claim 3] A plasma display system comprising: a panel section having a substrate formed with a plurality of scanning electrodes and sustaining electrodes in pairs and a substrate formed with data electrodes disposed perpendicularly of the scanning electrodes and sustaining electrodes, in

which the substrates are opposed to each other, and a drive unit which outputs a driving voltage for driving the panel section, wherein waveforms of the driving voltage include a sustaining period of alternately applying a sustaining pulse voltage for sustaining discharge to the scanning electrode and the sustaining electrode, and voltage Vsh (V) of sustaining pulse voltage finally applied has a relationship with voltage Vst (V) of sustaining pulse voltage previously applied and discharge start voltage Vf2 (V) between scanning electrode and sustaining electrode such as follows:

$Vst \leq sh < Vf2$

[Claim 4] The plasma display system of claim 3, wherein voltage Vsh (V) of final sustaining pulse voltage has a relationship with discharge start voltage Vf2 (V) between scanning electrode and sustaining electrode such as follows:

$(Vf2 - 50) \leq Vsh < (Vf2 - 30)$

[Claim 5] A plasma display system comprising: a panel section having a substrate formed with a plurality of scanning electrodes and sustaining electrodes in pairs and a substrate formed with data electrodes disposed perpendicularly of the scanning electrodes and retaining electrodes, in which the substrates are opposed to each other, and a drive unit which outputs a driving voltage for driving the panel section, wherein waveforms of the driving voltage include a sustaining period of alternately applying a sustaining pulse voltage for sustaining discharge to the scanning electrode and the sustaining electrode, and pulse width ts2 of final sustaining pulse voltage is greater than pulse width ts1 of previous sustaining pulse voltage.

[Claim 6] The plasma display system of claim 5, wherein pulse width ts2

(μs) of sustaining pulse voltage finally applied has a relationship with pulse width ts1 (μs) of sustaining pulse voltage previously applied such as follows:

$$(ts1 + 2) \leq ts2 \leq 20$$

[Claim 7] The plasma display system of claim 3 or 5, wherein waveforms of the driving voltage further include an erasing period of applying an oblique waveform voltage different in polarity from final sustaining pulse voltage to an electrode different from the electrode to which the final sustaining voltage is applied after the sustaining period.

[Claim 8] The plasma display system of claim 1 or 7, wherein inclination of the oblique waveform voltage in the erasing period ranges from 0.5 V/μs to 20 V/μs.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a plasma display system which is known as a thin, light-weight display system having a large screen.

[0002]

[Background Art]

In a plasma display system, ultraviolet ray is generated by gas discharge, and the ultraviolet ray excites a fluorescent material to emit light for color display.

[0003]

A plasma display system can be roughly classified into two types such as AC type and DC type in terms of drive, and surface discharge type and opposed discharge type in terms of discharge. For the manufacturing

convenience to cope with the requirements for highly precise, finer and larger screens, and more simplified structures, mainly manufactured at present is a plasma display system of surface discharge type having a three-electrode structure. A general structure of the panel section of the plasma display system is shown in Fig. 7.

[0004]

Scanning electrode 2 and sustaining electrode 3 are disposed distance MG (hereinafter referred to as main discharge gap MG) apart from each other on substrate 1 which is clear and insulative like glass, and further, scanning electrode 2 and sustaining electrode 3 in pairs are disposed distance IPG (hereinafter referred to as adjacent discharge cell gap IPG) apart from each other on the substrate. And, dielectric layer 4 and protective layer 5 are disposed so as to cover scanning electrode 2 and sustaining electrode 3. Also, a plurality of data electrodes 7 are installed on substrate 6 which is insulative like glass, and dielectric layer 8 is disposed so as to cover data electrodes 7. And, partition wall 9 is disposed in parallel with data electrode 8 on dielectric layer 8 between data electrodes 7. Fluorescent material 10 is arranged at the surface of dielectric layer 8 and the side of partition wall 9. And, substrate 1 and substrate 6 are disposed opposite to each other so that scanning electrode 2 and sustaining electrode 3 are perpendicular data electrodes 7, and the portion where scanning electrode 2 and sustaining electrode 3 in pairs intersect data electrode 7 is discharge cell 11. At least one of helium, neon, and argon and xenon are sealed as discharge gas into discharge cell 11.

[0005]

The schematic configuration of a drive unit which outputs a driving voltage for driving the panel section shown in Fig. 7 and the connection to each electrode of the panel section are shown in Fig. 8. The arrangement of each electrode of the panel section is of matrix configuration of mXn, and m columns of data electrodes 7 for addressing are arranged in the direction of column, and n columns of scanning electrodes 2 and sustaining electrodes 3 in pairs for sustaining discharge are arranged in the direction of row.

[0006]

The drive unit includes data-writing drive circuit 12, scanning drive circuit 13, initializing circuit 14, and sustaining drive circuit 15. Data-writing drive circuit 12 is a circuit for outputting a driving voltage to data electrodes 7, which is connected to each of data electrodes 7 by m pieces of output terminals. Also, scanning drive circuit 13 is a circuit for outputting a driving voltage to scanning electrodes 2, which is connected to each of scanning electrodes 2 by n pieces of output terminals. And, sustaining drive circuit 15 is a circuit for outputting a driving voltage to sustaining electrodes 3, which is connected in common to sustaining electrodes 3. Initializing circuit 14 is a circuit for executing initializing operation to accumulate the initial charge in each electrode having no charge accumulated before activation.

[0007]

Fig. 9 shows the waveform of driving voltage outputted from the drive unit. The driving voltage waveform shown in Fig. 9 shows an initializing period for accumulating the initial charge in each electrode having no charge accumulated before activation and a one-field period thereafter.

[0008]

The one-field period is a waveform for displaying one screen, and for example, it comprises a plurality of sub-fields ranging from No. 1 to No. 8. And, one sub-field comprises a wall voltage adjusting period, writing period, sustaining period, and erasing period. The operation during each of these periods will be described in the following.

[0009]

First, the operation during the initializing period is described. In the initializing period, all data electrodes D1~Dm and all scanning electrodes SCN1~SCNn are kept at 0 (V), and a positive waveform driving voltage rapidly increasing from 0 (V) up to potential Vpu (V) lower than the discharge start voltage with respect to all scanning electrodes SCN1~SCNn, followed by slowly increasing up to potential Vru (V) exceeding the discharge start voltage is applied to all sustaining electrodes SUS1~SUSn. While the voltage is slowly increased, in each of discharge cells 11, slight initializing discharge takes place first time from all sustaining electrodes SUS1~SUSn toward all data electrodes D1~Dm and all scanning electrodes SCN1~SCNn, then negative wall voltage is accumulated on the surface of protective layer 5 on sustaining electrodes SUS1~SUSn, and positive wall voltage is accumulated at the surface of fluorescent material 10 on data electrodes D1~Dm and the surface of protective layer 5 on scanning electrodes SCN1~SCNn. And in this condition, the potentials of all sustaining electrodes SUS1~SUSn are lowered toward 0 (V) at such a low speed that no discharge takes place between the electrodes. Thus, the initializing operation during the initializing period is completed.

[0010]

Next, the operation during the wall voltage adjusting period is described. In the wall voltage adjusting period, 0 (V) is applied to all sustaining electrodes SUS1~SUSn and all data electrodes D1~Dn, and positive waveform driving voltage slowly increasing from 0 (V) toward Vrc (V) is applied to all scanning electrodes SCN1~SCNn. While the voltage is slowly increased, in all discharge cells 11, slight discharge takes place with all sustaining electrodes SUS1~SUSn being negative and all scanning electrodes SUN1~SUNn being positive, and the positive wall voltage at the surface of protective layer 5 on all scanning electrodes SCN1~SCNn and the negative wall voltage at the surface of protective layer 5 on sustaining electrode SUSi are once adjusted to wall voltages suited for writing operation in the writing period which is executed after the wall voltage adjusting period. Subsequently, after 0 (V) is further applied to all scanning electrodes SCN1~SCNn, a driving voltage with waveforms of slowly decreasing toward Vns (V) is applied, and at the same time, a driving voltage with waveforms of slowly increasing from 0 (V) to Ve (V) is applied to all sustaining electrodes SUS1~SUSn. During the application of the voltages, slight discharge takes place with all sustaining electrodes SUS1~SUSn and all data electrodes D1~Dm being positive and all scanning electrodes SCNi being negative, and the positive wall voltage at the surface of fluorescent material 10 on all data electrodes D1~Dm and the negative wall voltage at the surface of protective layer 5 on all sustaining electrodes SUS1~SUSn and the positive wall voltage at the surface of protective layer 5 on all scanning electrodes SCN1~SCNn are adjusted to wall voltages

suited for writing operation in the writing period which is executed after the wall voltage adjusting period. Thus, the wall voltage adjusting period is completed.

[0011]

The operation in the writing period will be described in the following. During the writing period, potential Vsc (V) is applied to all scanning electrodes SCN1~SCNn, and potential Ve is successively applied to all sustaining electrodes SUS1~SUSn. Also, a writing pulse voltage of positive potential Vw (V) is applied to predetermined data electrode Dj (j stands for an integer ranging from 1 to m) corresponding to discharge cell 11 to be displayed in the first row out of data electrodes D1~Dm, and at the same time, negative polarity potential Vad (V) is applied to scanning electrode SCN1 in the first row. In this case, the potential difference between the surface of fluorescent material 10 and the surface of protective layer 5 on scanning electrode SCN1 at the intersection (first intersection) between specified data electrode Dj and scanning electrode SCN1 corresponds to the value obtained by subtracting the negative wall voltage at the surface of protective layer 5 on scanning electrode SCN1 from the value obtained by adding the positive wall voltage at the surface of fluorescent material 10 on data electrode Dj to data waveform potential Vw (that is, addition of absolute values), and therefore, at the first intersection, writing discharge takes place between specified data electrode Dj and scanning electrode SCN1. Simultaneously, due to the writing discharge, writing discharge also takes place between sustaining electrode SUS1 and scanning electrode SCN1 at the first intersection, then positive wall voltage

is accumulated at the surface of protective layer 5 on scanning electrode SCN1 at the first intersection, and negative wall voltage is accumulated at the surface of protective layer 5 on sustaining electrode SUS1 at the first intersection.

[0012]

Similar operations are successively performed up to the nth row to complete the writing operation in the writing period.

[0013]

Next, the operation in the sustaining period will be described. During the sustaining period, sustaining waveforms of potential Vst (V) are alternately applied to all scanning electrodes SCN1~SCNn and all sustaining electrodes SUS1~SUSn, and thereby, sustaining discharge continuously takes place at discharge cell 11 subjected to writing discharge. Visible ray emitted from fluorescent material 10 excited by ultraviolet ray generated due to the sustaining discharge is used for display.

[0014]

Here, the state of wall voltage of scanning electrode SCNi and sustaining electrode SUSi of discharge cell 11 where sustaining discharge successively takes place is as described in the following. First, when Vst (V) is applied to scanning electrode SCNi, and 0 (V) to sustaining electrode SUSi, then discharge takes place from scanning electrode SCNi toward sustaining electrode SUSi. Correspondingly, positive ion moves from scanning electrode SCNi toward sustaining electrode SUSi, and electron moves from sustaining electrode SUSi toward scanning electrode SCNi. Consequently, the wall voltage at the surface of protective layer 5 on

sustaining electrode SUSi becomes positive, and the wall voltage at the surface of protective layer 5 on scanning electrode SCNi becomes negative. And the moment next, the application of sustaining pulse voltage Vst (V) is switched, and when 0 (V) is applied to scanning electrode SCNi, and Vh (V) to sustaining electrode SUSi, then discharge takes place from sustaining electrode SUSi toward scanning electrode SCNi. Correspondingly, positive ion and electron make similar movement, and then the wall voltage at the surface of protective layer 5 on sustaining electrode SUSi changes from positive to negative, while the wall voltage at the surface of protective layer 5 on scanning electrode SCNi changes from positive to negative. And after repetition of the above operation, the sustaining discharge is completed with Vst (V) applied to sustaining electrode SUSi and 0 (V) applied to scanning electrode SCNi. At the time, the wall voltage at the surface of protective layer 5 on sustaining electrode SUSi change from positive to negative, and the wall voltage at the surface of protective layer 5 on scanning electrode SCNi changes from negative to positive. In the above condition, the operation in the sustaining period is completed.

[0015]

The operation in the erasing period is described in the following. During the erasing period, a driving voltage of waveforms slowly increasing from 0 (V) to potential Vd (V) is applied to all scanning electrodes SCN1~SCNn. In discharge cell 11 subjected to sustaining discharge, while the waveform voltage slowly increases, slight erasing discharge takes place between sustaining electrode SUSi (i stands for an integer ranging from 1 to n) and scanning electrode SCNi, then the positive wall voltage at the

surface of protective layer 5 on scanning electrode SCNi and the negative wall voltage at the surface of protective layer 5 on sustaining electrode SUSi weaken, causing the discharge to stop. Thus, the erasing operation in the erasing period is completed.

[0016]

And, the operation in the sub-field period starting from the wall voltage adjusting period is again repeated, and thereby, one-field period is configured to display the picture.

[0017]

[Problems to be Solved by the Invention]

However, in the plasma display system having the above-mentioned panel section and drive unit, there arises a problem of false discharge generated with the discharge cell pitch reduced because of being precise and fine in particular with respect to direction Y at the panel section shown in Fig. 7.

[0018]

The cause is probably the following mechanism. For example, the state of wall voltage at the surface of protective layer 5 on scanning electrode SCNi after application of final sustaining discharge must be such that the mode has been switched from negative to positive as describe earlier, and this can be realized with positive ion reaching the surface of protective layer 5. However, moving speed μ ion of positive ion is very slow as compared with moving speed μ e of electron, and therefore, for example, the changeover in the vicinity of main discharge gap MG is easily performed because the moving distance of positive ion is short, but the changeover at

the outside of scanning electrode SCNi requiring a long moving distance for positive ion, that is, in the vicinity of adjacent discharge cell gap IPG involves a problem of high probability of non-arrival of positive ion, and as a result, negative charge 16 is not neutralized and left at the outside of scanning electrode SCNi, that is, in the vicinity of adjacent discharge cell gap IPG. The condition is shown in Fig. 10 (a). Fig. 10 is an arrow view of Z-Z section in Fig. 7, where "+" and "–" stand for charge, but these are just conceptual and the numerals are not based on strict specifications.

[0019]

And, if the operations in the erasing period and wall voltage adjusting period thereafter are performed while negative charge 16 is remaining, wall voltage adjustment will be made as described earlier, but unneeded negative charge 16 still remains in the vicinity of adjacent discharge cell gap IPG.

[0020]

And in this condition, when scanning pulse voltage Vad (V) is applied to scanning electrode SCNi, and writing pulse voltage Vw (V) to data electrode Di, through the writing operation in the writing period, discharge 17 is generated (Fig. 10 (b)) between unnecessary negative charge 16 remaining in the vicinity of adjacent discharge cell gap IPG and data electrode Di, and due to the discharge 17, a large quantity of priming particles (semi-stable atom, ion, etc.) is simultaneously generated. Since the discharge 17 is generated in the vicinity of adjacent discharge cell gap IPG, the priming particles then generated are easy to get into the adjacent discharge cell, which is remarkable in case of narrow pitches of discharge

cells 11 because of being precise and fine. And, in Y direction shown in Fig. 7, nothing is disposed to physically restrict the discharge area such as partition wall 9 in X direction, and therefore, priming particles mainly flow into adjacent discharge cells in Y direction, and the priming particles cause the wall voltage of discharge cell 11 to change, and as a result, there arises a problem of false discharge such as wrong writing or defective writing in Y direction.

[0021]

The present invention is intended to solve the above problem, and the object is to obtain a plasma display system capable of stable picture display while suppressing false discharge even in case of a highly precise and fine discharge cell structure.

[0022]

[Means to Solve the Problems]

In order to achieve the above purpose, the plasma display system of the present invention is a plasma display system comprising a panel section having a substrate with scanning electrodes and sustaining electrodes formed in parallel to each other and a substrate with data electrodes formed perpendicularly of the scanning electrodes and retaining electrodes, in which the substrates are opposed to each other, and a drive unit which outputs a driving voltage for driving the panel section, wherein waveforms of the driving voltage include a sustaining period of alternately applying a sustaining pulse voltage for sustaining discharge to the scanning electrode and the sustaining electrode and an erasing period of applying an oblique waveform voltage different in polarity from the sustaining pulse voltage to

an electrode different from the electrode to which final sustaining pulse voltage is applied.

[0023]

Also, in order to achieve the above purpose, the plasma display system of the present invention is a plasma display system comprising a panel section having a substrate with scanning electrodes and sustaining electrodes formed in parallel to each other and a substrate with data electrodes formed perpendicularly of the scanning electrodes and sustaining electrodes, in which the substrates are opposed to each other, and a drive unit which outputs a driving voltage for driving the panel section, wherein waveforms of the driving voltage include a sustaining period of alternately applying a sustaining pulse voltage for sustaining discharge to the scanning electrode and the sustaining electrode, and voltage Vsh (V) of sustaining pulse voltage finally applied has a relationship with voltage Vst (V) of sustaining pulse voltage previously applied and discharge start voltage Vf2 (V) between scanning electrode and sustaining electrode such as follows:

$$Vst \leq sh < Vf2$$

[0024]

Also, in order to achieve the above purpose, the plasma display system of the present invention is a plasma display system comprising a panel section having a substrate with scanning electrodes and sustaining electrodes formed in parallel to each other and a substrate with data electrodes formed perpendicularly of the scanning electrodes and retaining electrodes, in which the substrates are opposed to each other, and a drive unit which outputs a driving voltage for driving the panel section, wherein

waveforms of the driving voltage include a sustaining period of alternately applying a sustaining pulse voltage for sustaining discharge to the scanning electrode and the sustaining electrode, and pulse width ts2 of sustaining pulse voltage finally applied is greater than pulse width ts1 of sustaining pulse voltage previously applied.

[0025]

According to the above configuration, it is possible to obtain a plasma display system capable of stable picture display while suppressing false discharge even in case of a highly precise and fine discharge cell structure.

[0026]

[Description of the Preferred Embodiments]

(First preferred embodiment)

One preferred embodiment of the present invention will be described in the following with reference to the drawings. Incidentally, the panel section in this preferred embodiment is same as the panel section shown in Fig. 7, and the schematic configuration of the drive unit which outputs a driving voltage for driving the panel section and the connection to each electrode of the panel section are same as those shown in Fig. 8. Accordingly, the description is omitted here.

[0027]

Fig. 1 shows the waveforms of driving voltage outputted from the drive unit for driving the panel section, showing an initializing period for accumulating the initial charge for each electrode having no charge accumulated before activation, and one sub-field period thereafter.

[0028]

One field period is a waveform for displaying one screen, and for example, it comprises a plurality of sub-fields ranging from 1st to 8th. And, one sub-field comprises a wall voltage adjusting period, writing period, sustaining period, and erasing period. The difference of the present preferred embodiment from the prior art is such that after the end of sustaining period there is provided an erasing period of applying an oblique waveform voltage different in polarity from sustaining pulse voltage to an electrode different from the electrode to which the final sustaining pulse voltage is applied.

[0029]

The operation during the sustaining period and possible actions will be described in the following. In the erasing period, data electrode Di is kept at Vrd (V), and sustaining electrode SUSi is kept at 0 (V), and in this condition, an oblique waveform voltage slowly decreasing toward Vnr (V) is applied to scanning electrode SCNi. Then, while the oblique waveform voltage is decreasing, as shown in Fig. 2, slight discharge 18 is generated with data electrode Di being positive and scanning electrode SCNi being negative, and unnecessary negative charge 16 remaining on protective layer 5 on scanning electrode SCNi is erased, and thereby, it is possible to suppress the generation of false discharge. Here, Fig. 2 is an arrow view of Z-Z section in Fig. 7.

[0030]

As described above, since there is provided an erasing period of applying an oblique waveform voltage different in polarity from sustaining pulse voltage to an electrode different from the electrode to which the final

sustaining pulse voltage is applied, it becomes possible to suppress the generation of false discharge. Accordingly, it is possible to obtain a plasma display system capable of stable picture display even in case of a high precise and fine discharge cell structure.

[0031]

In the above description, the scanning electrode is A and the sustaining electrode is B, then the repetition of arrangement in substrate 1 is ABAB in the example. Besides the example, similar effect can be obtained for example in ABBA arrangement where same type of electrode is disposed between adjacent cells. In this case, due to increase in the number of discharge cells to meet the requirement for being highly precise and fine, electrostatic capacity between electrodes at the panel section is increased causing reactive power to increase in the ABAB arrangement, but electrostatic capacity at adjacent cell gap can be decreased in the ABBA arrangement, thereby suppressing the generation of reactive power, and it is possible to obtain an effect of suppressing the power consumption of the plasma display system.

[0032]

Also, when minimum voltage Vnr (V) of oblique waveform voltage applied during the erasing period has a relationship with discharge start voltage Vf1 (V) between data electrode Di and scanning electrode SCNi such as $-(Vf1 - 60) \leq Vnr \leq -30$, it is preferable because the effect of the present preferred embodiment will be further enhanced.

[0033]

(Second preferred embodiment)

Another preferred embodiment of the present invention will be described in the following with reference to the drawings. Incidentally, the panel section in this preferred embodiment is same as the panel section shown in Fig. 7, and the schematic configuration of the drive unit which outputs a driving voltage for driving the panel section and the connection to each electrode of the panel section are same as those shown in Fig. 8. Accordingly, the description is omitted here, and the difference of the present preferred embodiment from the prior art will be described in the following by using Fig. 3.

[0034]

Fig. 3 shows the waveforms of driving voltage outputted from the drive unit for driving the panel section of the plasma display system of the present invention, showing a sustaining period, wall voltage adjusting period, and writing period.

[0035]

The difference of this preferred embodiment from the prior art is such that final sustaining pulse peak voltage Vsh (V) in the sustaining period has a relationship with previous sustaining pulse peak voltage Vst (V) and discharge start voltage Vf (V) such as $Vst < Vsh < Vf$.

[0036]

The resultant effect is probably as follows. Since the final sustaining pulse peak voltage Vsh (V) is greater than the previous sustaining pulse peak voltage Vst (V), the electrical attraction against positive ion becomes greater at the time of final sustaining discharge during the sustaining period, and therefore, positive ion may reach even at the outside of scanning

electrode SCNi requiring a long moving distance for positive ion, that is, in the vicinity of adjacent discharge cell gap IPG. As a result, the wall voltage at the surface of protective layer 5 on scanning electrode SCNi after application of final sustaining discharge is sufficiently changed from negative to positive, allowing no unneeded negative charge to remain, and thereby, it is possible to prevent the generation of false discharge.

[0037]

As described above, voltage Vsh (V) of final sustaining pulse voltage has a relationship with voltage Vst (V) of previous sustaining pulse voltage and discharge start voltage Vf2 (V) between scanning electrode and sustaining electrode such as $Vst \leq Vsh < Vf2$, and therefore, it becomes possible to suppress the generation of false discharge. Accordingly, it is possible to obtain a plasma display system capable of stable picture display even in case of a highly precise and fine discharge cell structure.

[0038]

Here, as shown in Fig. 4 as the waveform of driving voltage, it is preferable to add the waveform of diving voltage in the erasing period for erasing unneeded negative charge remaining in the vicinity of adjacent discharge cell gap IPG as shown in the first preferred embodiment to the waveform of driving voltage in the present preferred embodiment because it will be able to further enhance the effect of erasing unneeded negative charge.

[0039]

Also, when voltage Vsh (V) of final sustaining pulse voltage has a relationship with discharge start voltage Vf2 (V) between scanning electrode

and sustaining electrode such as $Vst \leq Vsh < Vf2$, or preferably $(Vf2 - 50) \leq Vsh < (Vf2 - 30)$, it is preferable because the effect of this embodiment will be further enhanced.

[0040]

(Third preferred embodiment)

Another preferred embodiment of the present invention will be described in the following with reference to the drawings. Incidentally, the panel section used in this preferred embodiment is same as the panel section shown in Fig. 7, and the schematic configuration of the drive unit which outputs a driving voltage for driving the panel section and the connection to each electrode of the panel section are same as those shown in Fig. 8. Accordingly, the description is omitted here, and the difference of the present preferred embodiment from the prior art will be described in the following by using Fig. 5.

[0041]

Fig. 5 shows the waveforms of driving voltage outputted from the drive unit for driving the panel section of the plasma display system in the present preferred embodiment, showing a sustaining period, wall voltage adjusting period, and writing period. The difference of this preferred embodiment from the prior art is such that pulse width ts2 (μs) of final sustaining pulse in the sustaining period is wider than pulse width ts1 (μs) of previous sustaining pulse.

[0042]

The resultant effect is probably as follows. Since pulse width ts2 of the final sustaining pulse voltage is greater than pulse width ts1 of the

previous sustaining pulse voltage, the moving time of positive ion becomes longer at the time of final sustaining discharge during the sustaining period, and therefore, positive ion may reach even at the outside of scanning electrode SCNi requiring a long moving distance for positive ion, that is, in the vicinity of adjacent discharge cell gap IPG. As a result, the wall voltage at the surface of protective layer 5 on scanning electrode SCNi is sufficiently changed from negative to positive, allowing no unneeded negative charge to remain, and thereby, it is possible to prevent the generation of false discharge.

[0043]

As described above, pulse width ts2 of the final sustaining pulse voltage is greater than pulse width ts1 of the previous sustaining pulse voltage, and therefore, it becomes possible to suppress the generation of false discharge. Accordingly, it is possible to obtain a plasma display system capable of stable picture display even in case of a highly precise and fine discharge cell structure.

[0044]

Here, as shown in Fig. 6 as the waveform of driving voltage, it is preferable to add the waveform of diving voltage in the erasing period for erasing unneeded negative charge remaining in the vicinity of adjacent discharge cell gap IPG as shown in the first preferred embodiment to the waveform of driving voltage in the present preferred embodiment because it will be able to further enhance the effect of erasing unneeded negative charge.

[0045]

Also, when pulse width ts2 (μs) of the final sustaining pulse in the sustaining period has a relationship with pulse width ts1 (μs) of the final sustaining pulse such as $(ts1 + 2) \leq ts2 \leq 20$, it is preferable because the effect in the present preferred embodiment will be further enhanced.

[0046]

Also, in the above description, a driving method in which the pulse width of final sustaining pulse in the sustaining period is greater than the pulse width of previous sustaining pulse is employed, but the present invention is not limited to this, and it is of course possible to obtain similar effects by using a driving method in which the pulse width of sustaining pulse after the second or third from the final one in the sustaining period is greater than the pulse width of previous sustaining pulse.

[0047]

Also, in the first to third preferred embodiments, maximum voltage Vrc (V) of oblique waveform voltage applied to the scanning electrode during the wall voltage adjusting period is preferable to have a relationship with discharge start voltage Vf1 (V) between data electrode Di and scanning electrode SCNi such as $(Vf1 - 50) \leq Vrc < Vf1$.

[0048]

In the first to third preferred embodiments, the gradient of each oblique waveform voltage in the erasing period and the wall voltage adjusting period is required to be moderate enough to obtain quick changeover and also to prevent the generation of unneeded discharge, and from this point of view, it is preferable to range from 0.5 V/μs to 20 V/μs.

[0049]

Also, as is obvious in the above description, scanning electrodes SCN1~SCNn and sustaining electrodes SUS1~SUSn are completely same at the panel section, which are discriminated from each other by the driving voltage applied. Accordingly, as to the waveform of driving voltage applied to scanning electrodes SCN1~SCNn and the waveform of driving voltage applied to sustaining electrodes SUS1~SUSn which are shown in the first to third preferred embodiments, it is of course possible to obtain similar effects even in case of changing places with each other.

[0050]

[Advantages of the Invention]

As is obvious in the above description, according to the plasma display system of the present invention, the waveform of driving voltage outputted from the drive unit includes an erasing period of applying an oblique waveform voltage different in polarity from the sustaining pulse voltage to an electrode different from the electrode to which the final sustaining pulse voltage is applied, and thereby, it will be able to erase unneeded charge remaining in the vicinity of adjacent discharge cell gap which causes false discharge, and as a result, false discharge can be suppressed.

[0051]

Accordingly, it is possible to obtain a plasma display system capable of stable picture display even in case of a highly precise and fine discharge cell structure.

[Brief Description of the Drawings]

Fig. 1 is a timing chart of driving voltage waveforms outputted from the drive unit of a plasma display system in one preferred embodiment of

the present invention.

Fig. 2 is a sectional view showing a state of charge in the panel section of a plasma display system in one preferred embodiment of the present invention.

Fig. 3 is a timing chart of driving voltage waveforms outputted from the drive unit of a plasma display system in another preferred embodiment of the present invention.

Fig. 4 is a timing chart of driving voltage waveforms outputted from the drive unit of a plasma display system, similarly, in another preferred embodiment of the present invention.

Fig. 5 is a timing chart of driving voltage waveforms outputted from the drive unit of a plasma display system, similarly, in another preferred embodiment of the present invention.

Fig. 6 is a timing chart of driving voltage waveforms outputted from the drive unit of a plasma display system, similarly, in another preferred embodiment of the present invention.

Fig. 7 is a sectional perspective view showing the structure of the panel section of a general plasma display system.

Fig. 8 is a diagram showing the schematic configuration of the drive unit and the connection to each electrode of the panel section of a general plasma display system.

Fig. 9 is a timing chart of the waveform of driving voltage outputted from the drive unit of a conventional plasma display system.

Fig. 10 is a sectional view showing a state of charge in the panel section of a conventional plasma display system.

[Description of the Reference Numerals and Signs]

2 Scanning electrode

3 Sustaining electrode

7 Data electrode

11 Discharge cell

12 Data writing drive circuit

13 Scanning drive circuit

14 Initializing circuit

15 Sustaining drive circuit

[Name of the Document] Abstract

[Abstract]

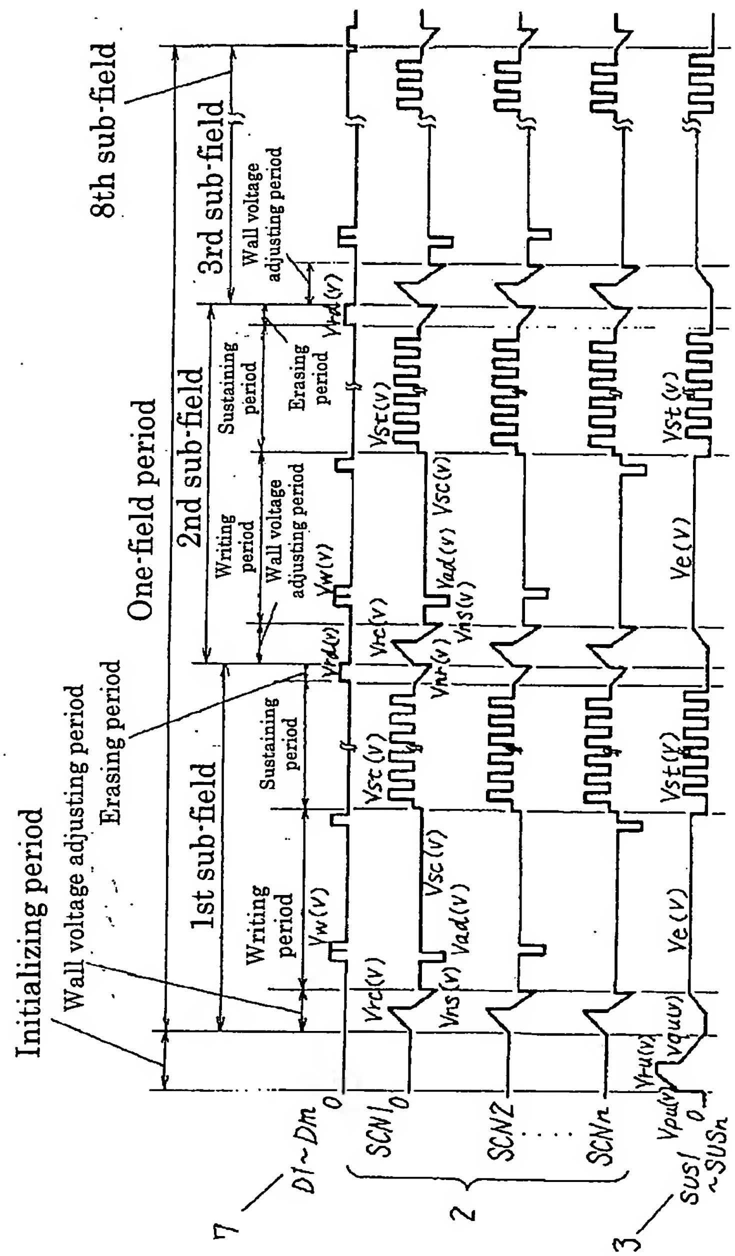
[Object] The object of the invention is to obtain a plasma display system capable of stable operation while suppressing false discharge with adjacent cells caused due to highly precise and fine configuration in the plasma display system.

[Means to Solve the Problem] The waveform of driving voltage outputted from the drive unit of the plasma display system includes a sustaining period of alternately applying a sustaining pulse voltage for sustaining discharge to the scanning electrode and sustaining electrode and an erasing period of applying an oblique waveform voltage different in polarity from the sustaining pulse voltage to an electrode different from the electrode to which the final sustaining pulse voltage is applied. In this configuration, it is possible to suppress false discharge and to obtain a plasma display system capable of stable picture display.

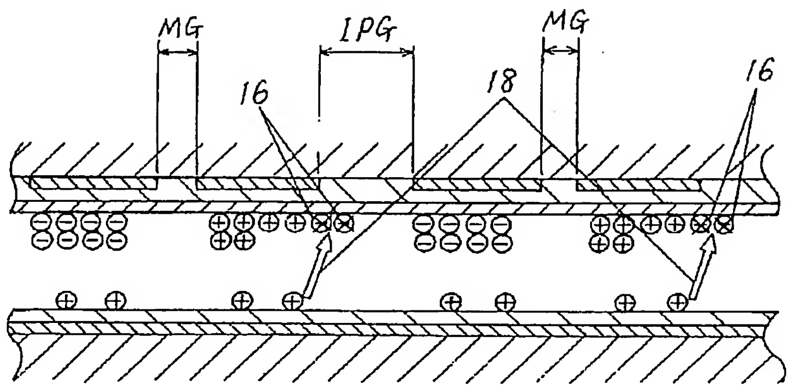
[Selected Drawing] Fig. 1

[Name of the Document] Drawings

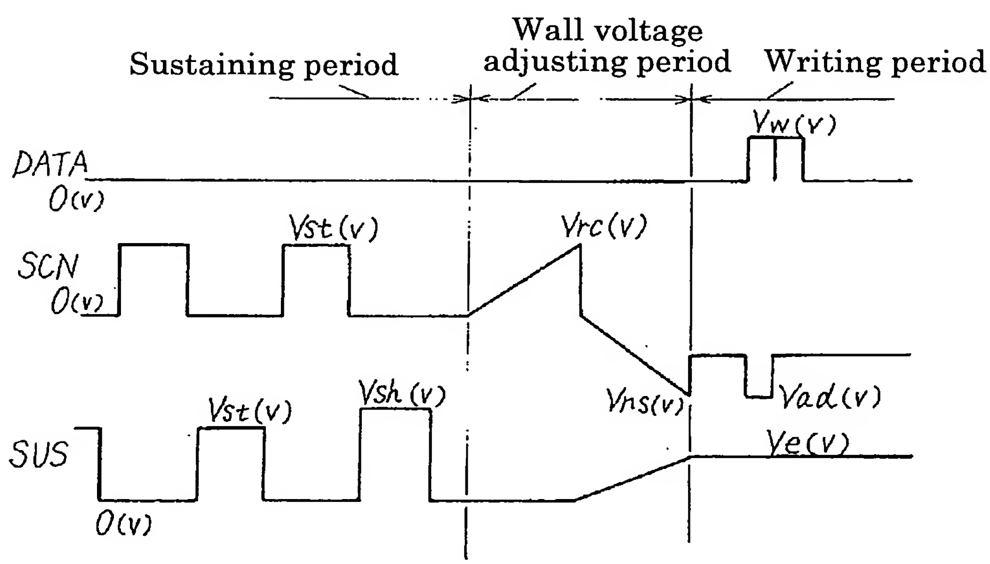
[Fig. 1]



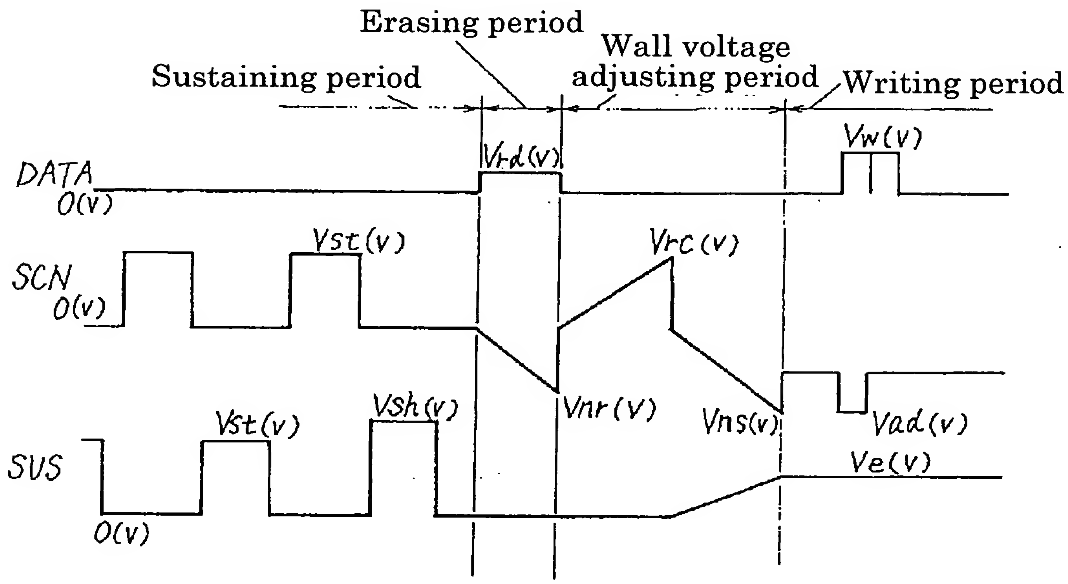
[Fig. 2]


MG
IPG
MG
16
18
16

[Fig. 3]

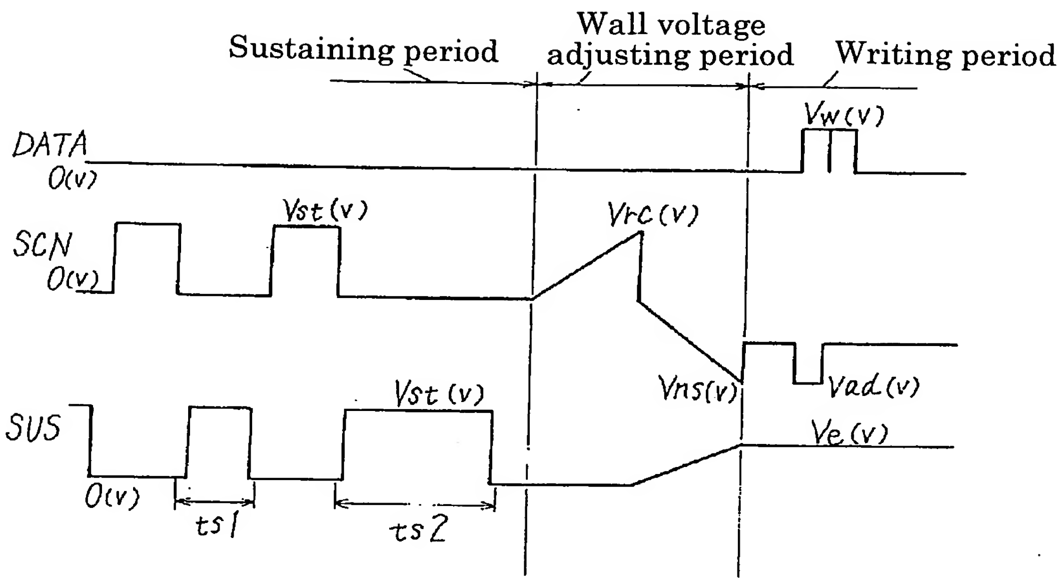

Sustaining period
Wall voltage
adjusting period
Writing period
DATA
0(v)
Vw(v)
SCN
0(v)
Vst(v)
Vrc(v)
Vns(v)
Vad(v)
SUS
0(v)
Vst(v)
Vsh(v)
Ve(v)

[Fig. 4]



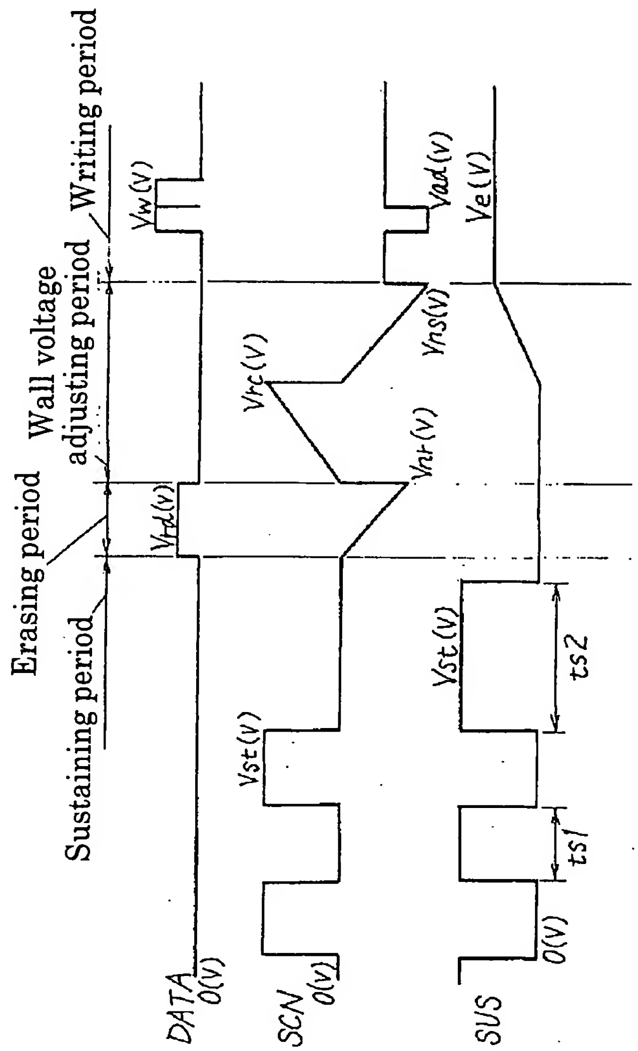
Erasing period
Wall voltage adjusting period
Sustaining period
Writing period
Vrd(V)
Vw(V)
DATA
0(V)
Vst(V)
Vrc(V)
SCN
0(V)
Vnr(V)
Vns(V)
Vad(V)
Vsh(V)
Vst(V)
SUS
Ve(V)
0(V)

[Fig. 5]



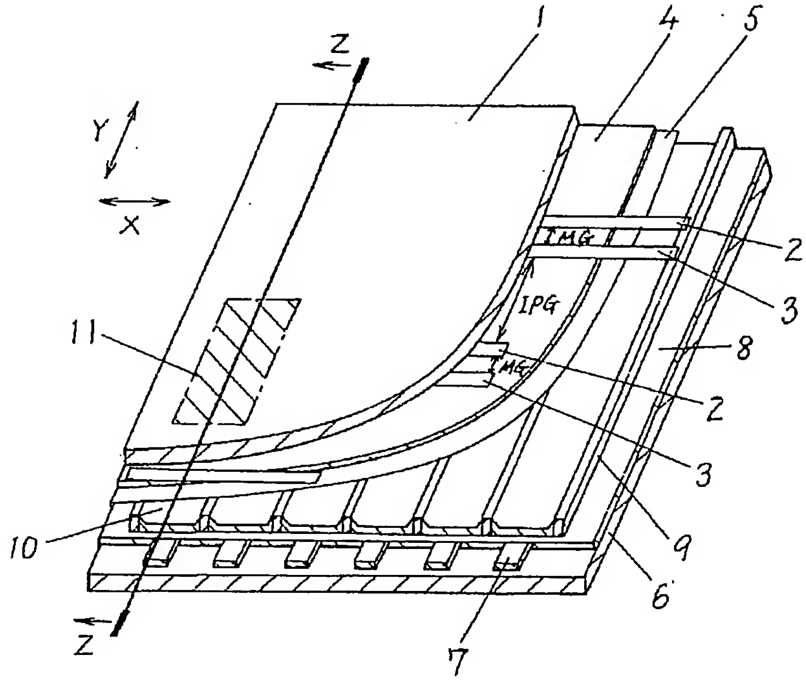
Sustaining period
Wall voltage adjusting period
Writing period
DATA
0(v)
Vw(v)
SCN
0(v)
Vst(v)
Vrc(v)
Vns(v)
Vad(v)
SUS
0(v)
Vst(v)
Ve(v)
ts1
ts2

[Fig. 6]

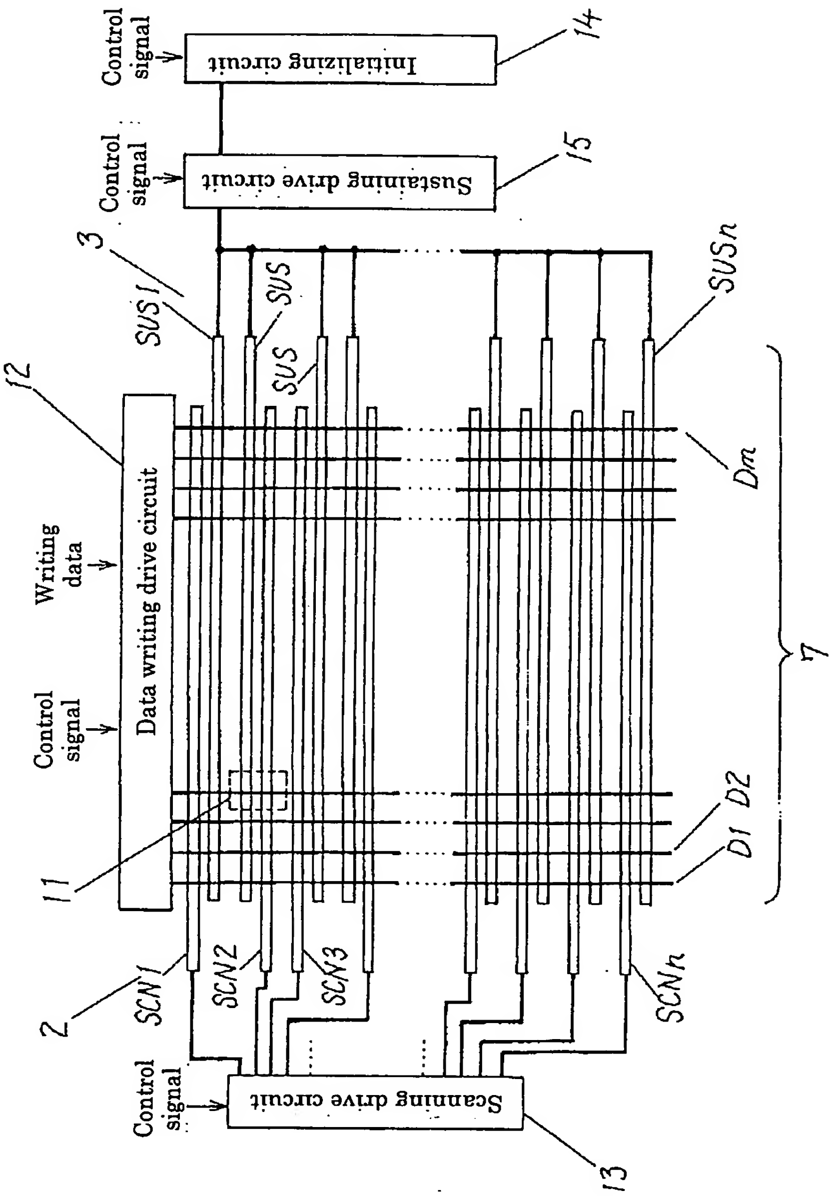


Writing period
Wall voltage adjusting period
Erasing period
Sustaining period
Vw(V)
Vad(V)
Ve(V)
Vrc(V)
Vns(V)
Vnr(V)
Vst(V)
Vst(V)
ts2
ts1
DATA
0(V)
SCN
0(V)
SUS
0(V)

[Fig. 7]

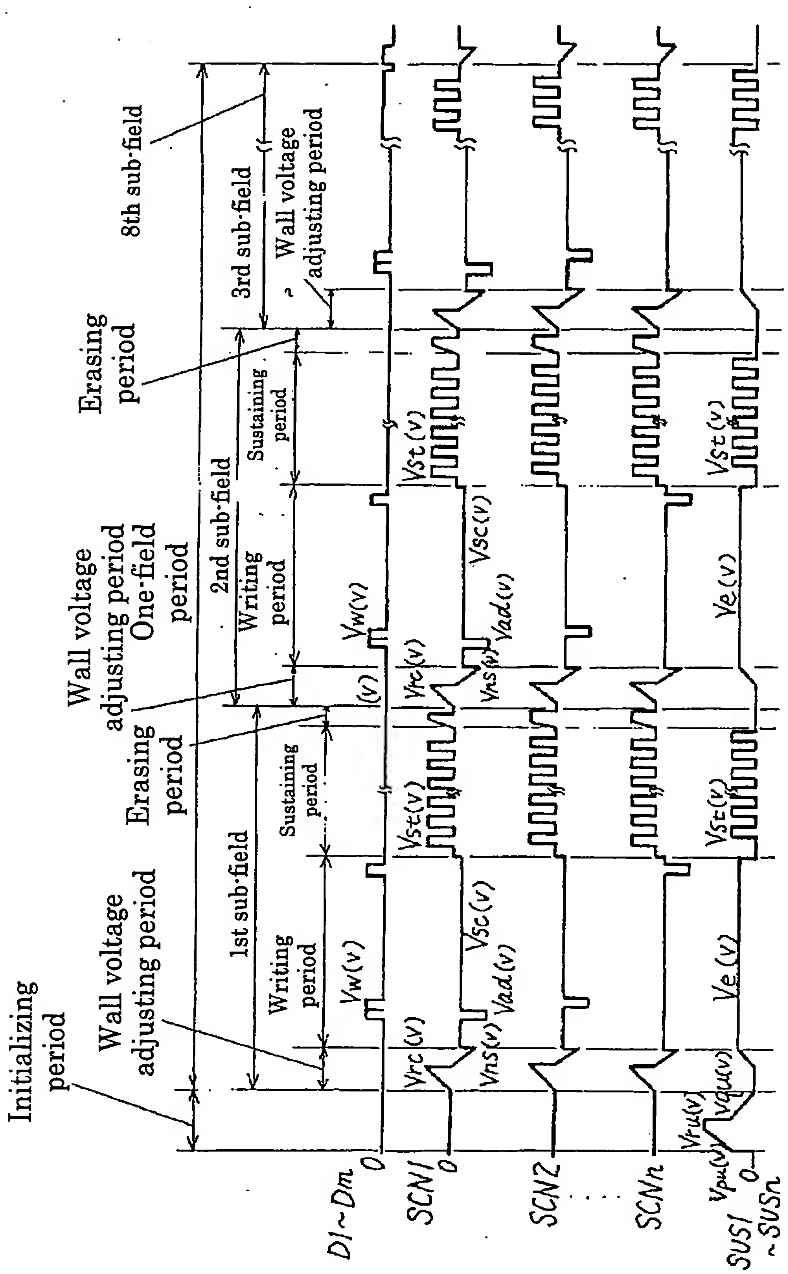


[Fig. 8]



Control signal
Initializing circuit
14
Control signal
Sustaining drive circuit
15
3
SUS1
SUS
SUS
SUSn
12
Writing data
Control signal
Data writing drive circuit
Dm
D2
D1
7
11
2
SCN1
SCN2
SCN3
SCNn
Control signal
Scanning drive circuit
13

[Fig. 9]



Initializing period
Wall voltage adjusting period
1st sub-field
Writing period
Sustaining period
Erasing period
Wall voltage adjusting period
One-field period
2nd sub-field
Writing period
Sustaining period
Erasing period
3rd sub-field
Wall voltage adjusting period
8th sub-field
D1~Dm
SCN1
SCN2
SCNn
SUS1 ~SUSn
Vw(v)
Vrc(v)
Vns(v)
Vad(v)
Vsc(v)
Vst(v)
Ve(v)
Vru(v)
Vpu(v)
Vqu(v)

[Fig. 10]